

Attorney Docket # 5367-219PUS



Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Volker HÄRLE et al.

Serial No.: 10/566,521

Filed: September 25, 2006

For: Method for the Production of a Plurality of
Opto-Electronic Semiconductor Chips and Opto-
Electronic Semiconductor Chip

Group Art: 1722

REQUEST FOR CORRECTION OF FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

Attached is a copy of the official filing receipt received from the U.S. Patent and
Trademark Office in the above-identified application.

There is an error in:

- ☐ Applicants' name and/or address
- ☐ Title
- ☐ Filing Date
- ☐ Serial Number
- ☐ Priority Data (country, number)
- ☒ Incorrect Priority Date
- ☐ Other [pls specify]

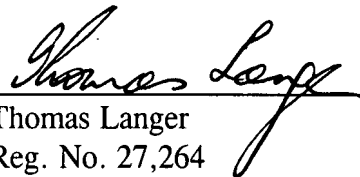
which should read as follows: **GERMANY 103 35 081.0 07/31/2003**

A copy of the filing receipt is submitted herewith on which the requested change is entered in red. We have also enclosed a copy of the PCT publication for your viewing upon correction.

It is respectfully requested that a corrected filing receipt be issued.

Respectfully submitted,
COHEN PONTANI LIEBERMAN & PAVANE LLP

By:



Thomas Langer
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Dated: August 6, 2007

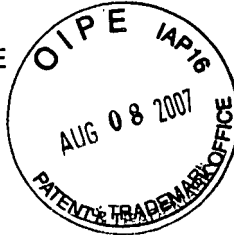


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APPL NO.	FILING OR 371(c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLMS	IND CLMS
10/566,521	09/25/2006	1722	1030	5367-219PUS	18	1

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CONFIRMATION NO. 7206

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Applicant(s)

Volker Harle, Waldetzenberg, GERMANY;

Power of Attorney: The patent practitioners associated with Customer Number 27799.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/DE04/01594 07/22/2004

Foreign Applications

GERMANY 103 35 081.0 07/30/2003 — 7/31/2003

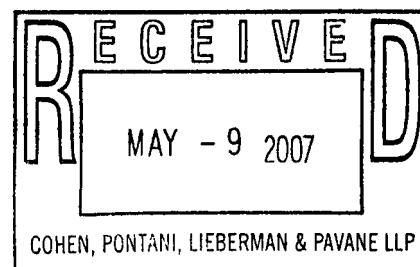
If Required, Foreign Filing License Granted: 05/04/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US10/566,521**

Projected Publication Date: 08/16/2007

Non-Publication Request: No

Early Publication Request: No



1077084800

Title

Method for the production of a plurality of opto-electronic semiconductor chips and opto-electronic semiconductor chip

Preliminary Class

117

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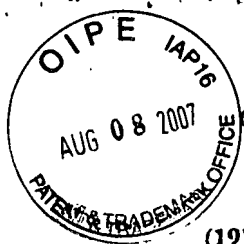
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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro



(43) Internationales Veröffentlichungsdatum
10. Februar 2005 (10.02.2005) ✓

PCT

(10) Internationale Veröffentlichungsnummer
WO 2005/013316 A3 ✓

(51) Internationale Patentklassifikation⁷: **H01L 21/20**, 33/00

(71) Anmelder (für alle Bestimmungsstaaten mit Ausnahme von US): **OSRAM OPTO SEMICONDUCTORS GMBH** (DE/DE); Wernerwerkstrasse 2, 93049 Regensburg (DE). ✓

(21) Internationales Aktenzeichen: **PCT/DE2004/001594** ✓

(22) Internationales Anmeldedatum:
22. Juli 2004 (22.07.2004) ✓

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(25) Einreichungssprache: **Deutsch**

(26) Veröffentlichungssprache: **Deutsch**

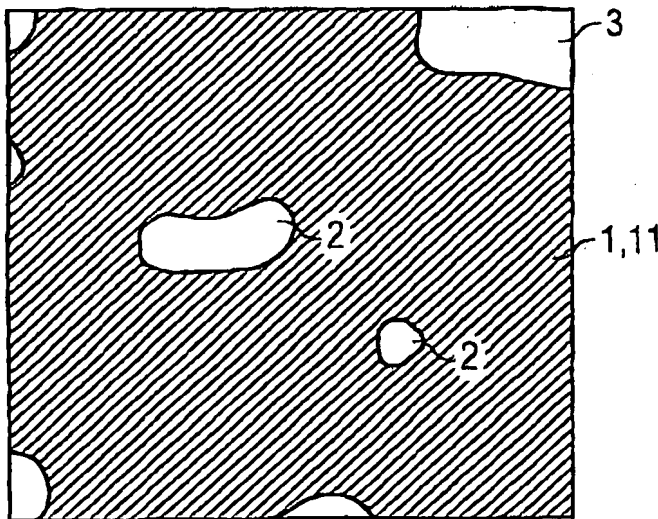
(74) Anwalt: **EPPING HERMANN FISCHER PATENTANWALTSGESELLSCHAFT MBH**; Ridlerstrasse 55, 80339 München (DE). ✓

(30) Angaben zur Priorität:
103 35 081.0 31. Juli 2003 (31.07.2003) DE ✓

[Fortsetzung auf der nächsten Seite]

(54) Title: METHOD FOR THE PRODUCTION OF A PLURALITY OF OPTO-ELECTRONIC SEMICONDUCTOR CHIPS AND OPTO-ELECTRONIC SEMICONDUCTOR CHIP

(54) Bezeichnung: VERFAHREN ZUR HERSTELLUNG EINER VIELZAHL VON OPTOELEKTRONISCHEN HALBLEITERCHIPS UND OPTOELEKTRONISCHER HALBLEITERCHIP ✓



(57) Abstract: The invention relates to a method for the production of a plurality of opto-electronic semiconductor chips respectively comprising a plurality of structural elements respectively consisting of at least one semiconductor layer. According to the inventive method, a chip composite base is produced, said base comprising a substrate and an epitaxial surface. A non-closed mask material layer is grown on the epitaxial surface. The mask material layer consists of a plurality of statistically distributed windows having various forms and/or opening surfaces. A masking material is selected in such a way that a semiconductor material of the semiconductor layer, which is grown in a later step of the inventive method, cannot grow on said material or grows in a substantially worse manner in comparison with the epitaxial surface. Subsequently, semiconductor layers are deposited on the epitaxial surface in an essentially simultaneous manner on areas located inside the windows. In another step of the inventive method, the chip composite base with deposited material is separated to form semiconductor chips. The

invention also relates to an optoelectronic semiconductor element produced according to said method.

(57) Zusammenfassung: Die Erfindung betrifft ein Verfahren zur Herstellung einer Vielzahl von optoelektronischen Halbleiterchips, die jeweils eine Vielzahl von Strukturelementen mit jeweils mindestens einer Halbleiterschicht aufweisen. Bei dem Verfahren wird eine Chipverbund-Basis bereitgestellt, die ein Substrat sowie eine Aufwachsfläche aufweist. Auf die Aufwachsfläche wird eine nicht geschlossene Maskenmaterialschicht derart aufgewachsen, dass die Maskenmaterialschicht eine Vielzahl statistisch verteilter Fenster mit variierenden Formen und/oder Öffnungsflächen aufweist, wobei ein Maskenmaterial derart gewählt ist, dass sich ein in einem späteren Verfahrensschritt aufzuwachsendes Halbleitermaterial auf diesem im Wesentlichen nicht oder im Vergleich zur Aufwachsfläche wesentlich schlechter aufwachsen lässt.

[Fortsetzung auf der nächsten Seite]

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